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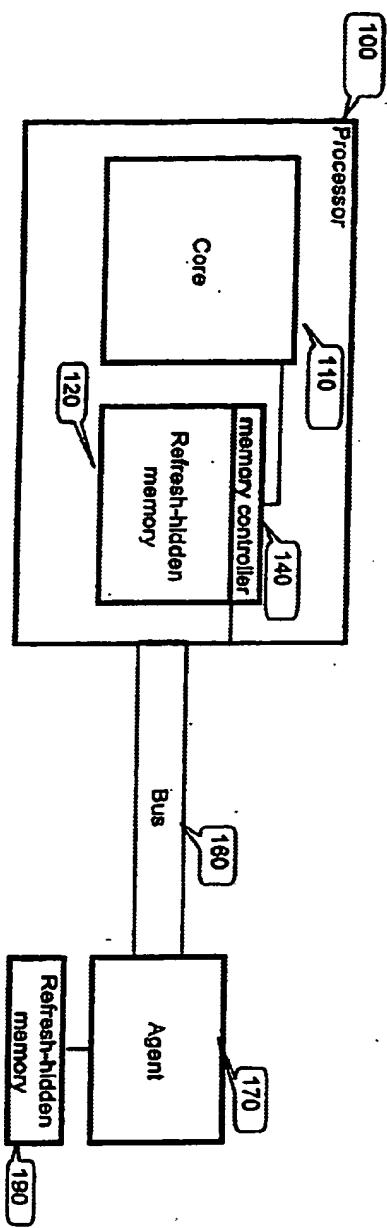


Figure 1

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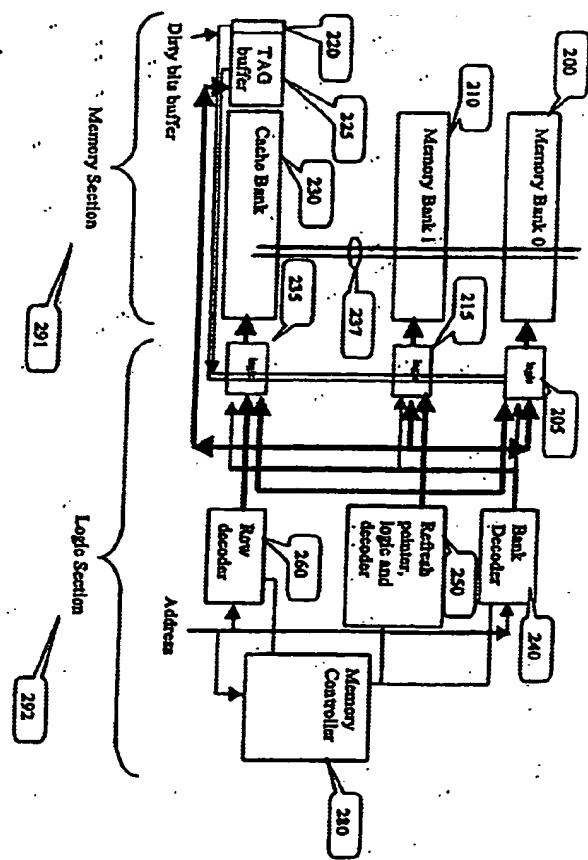
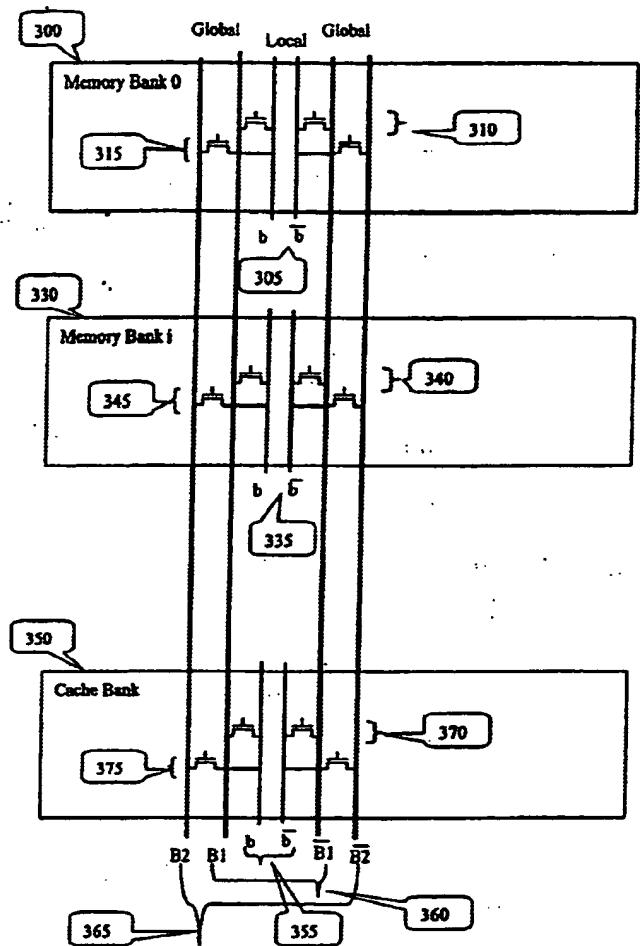


Figure 2

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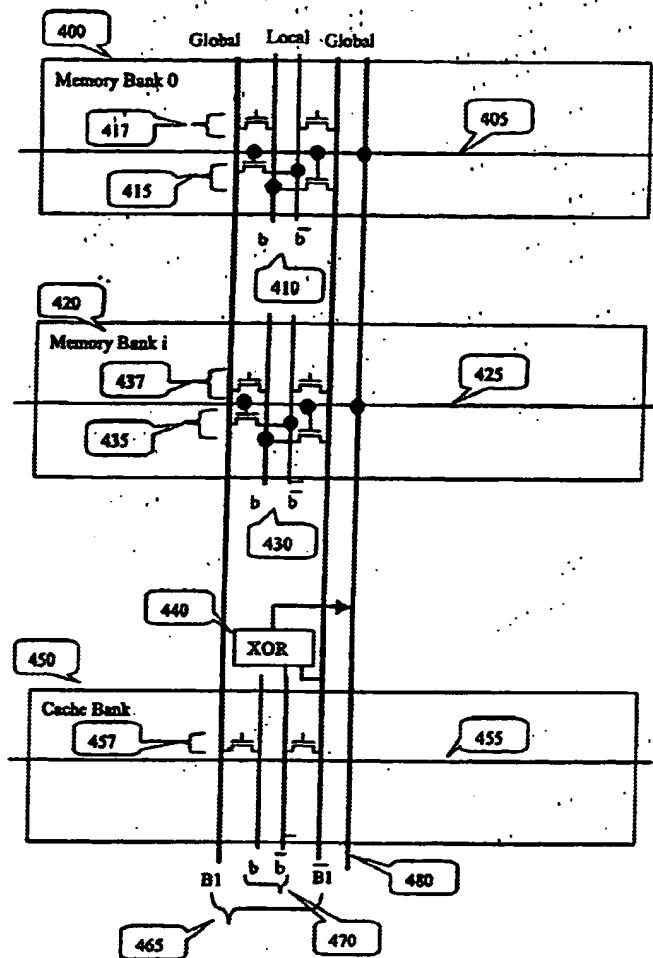
Figure 3



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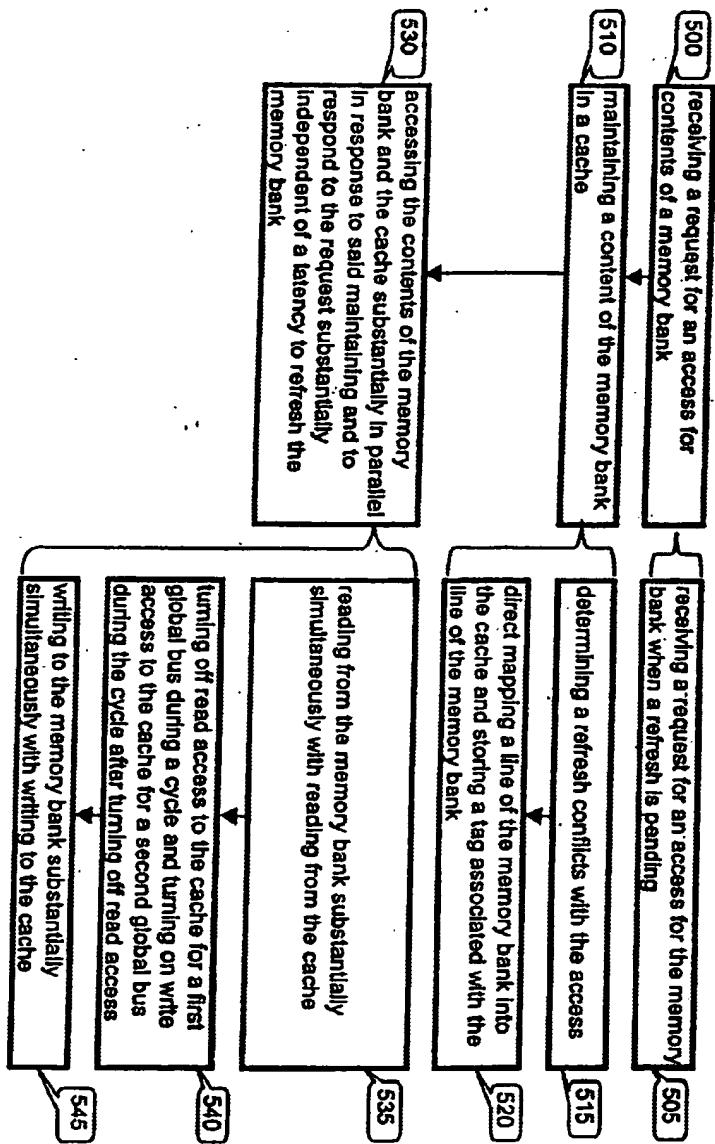
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Figure 4



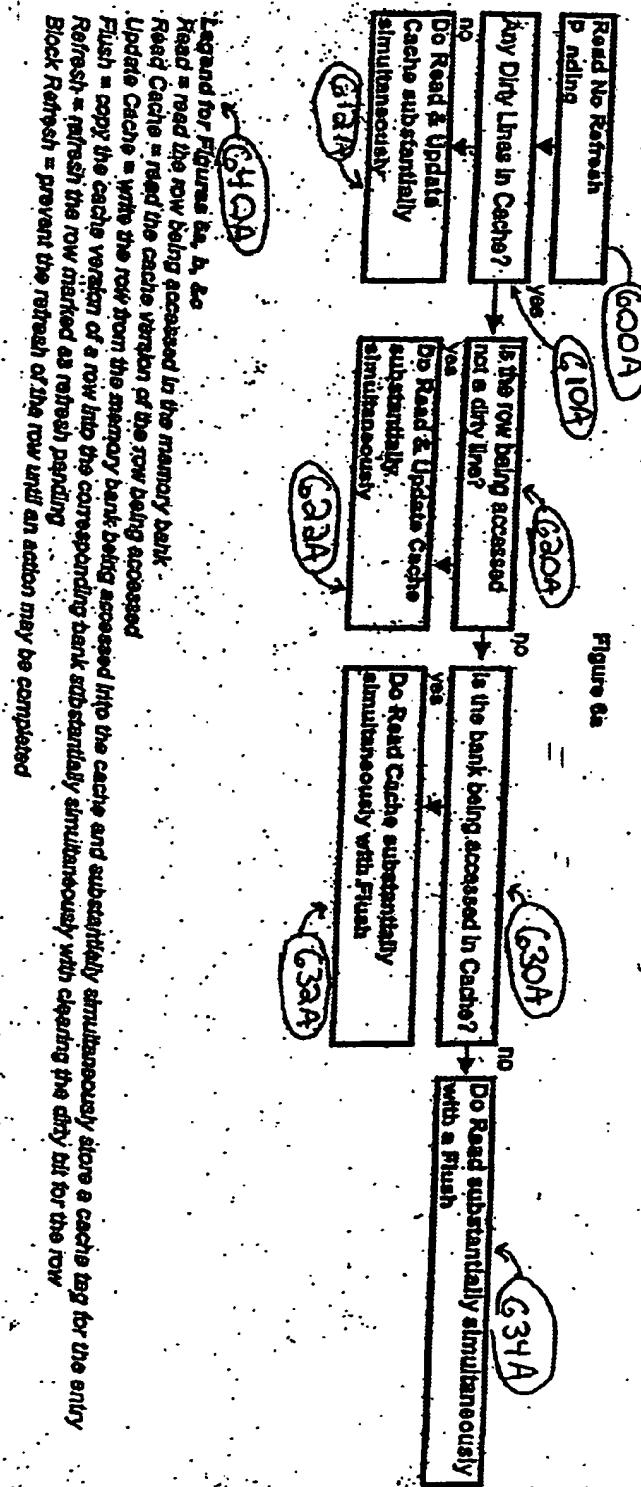
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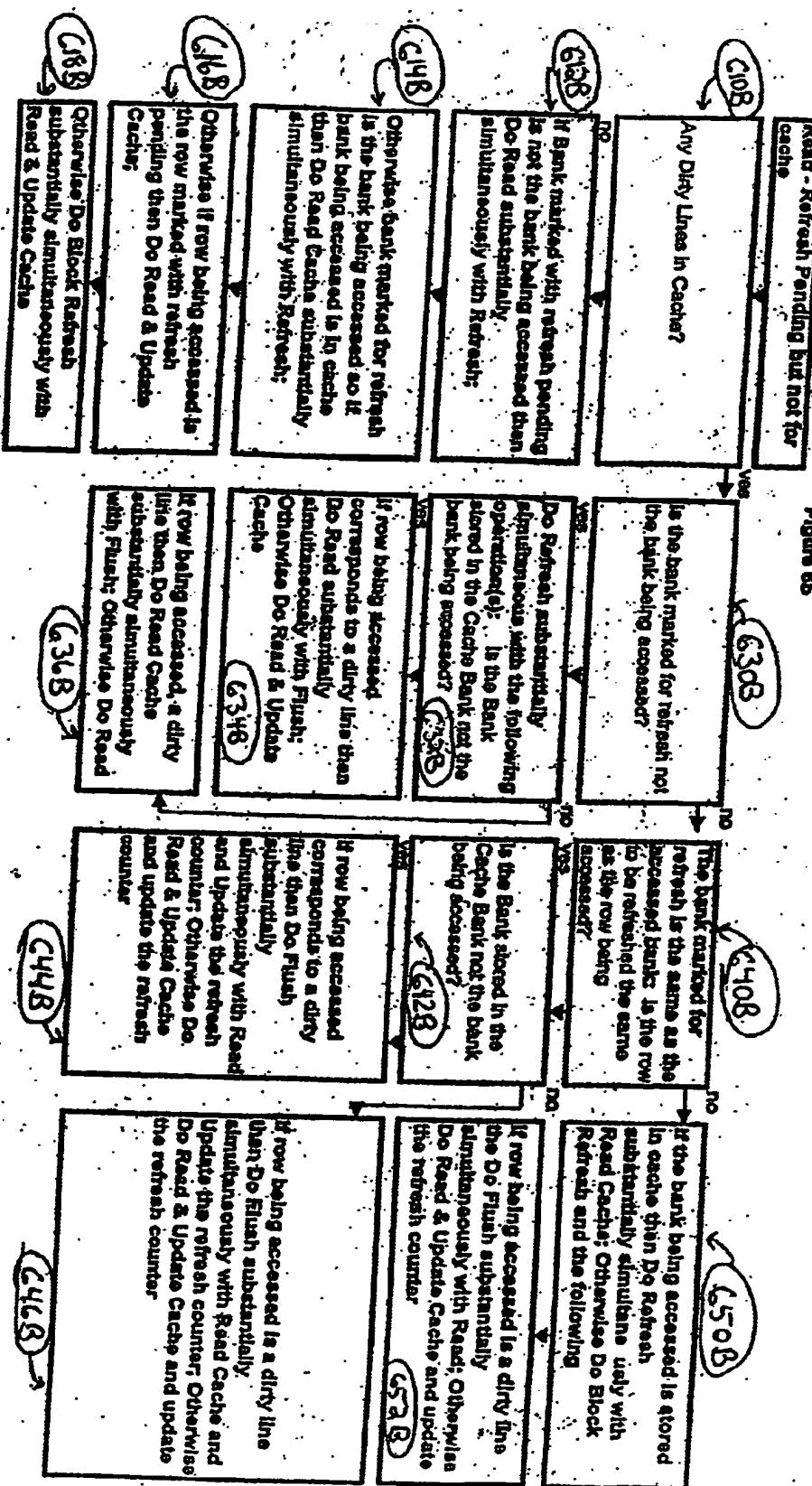
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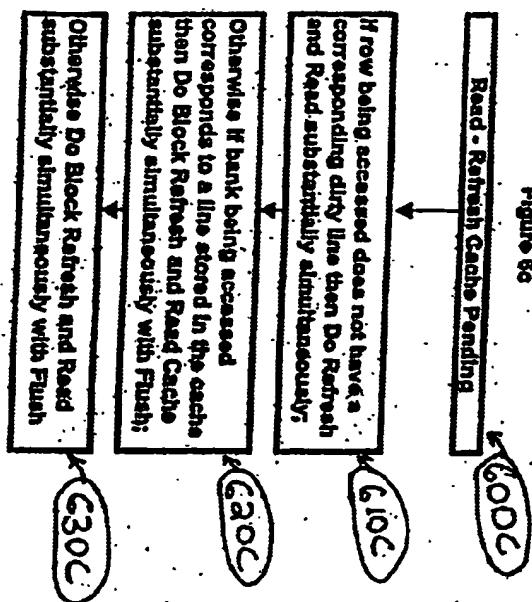
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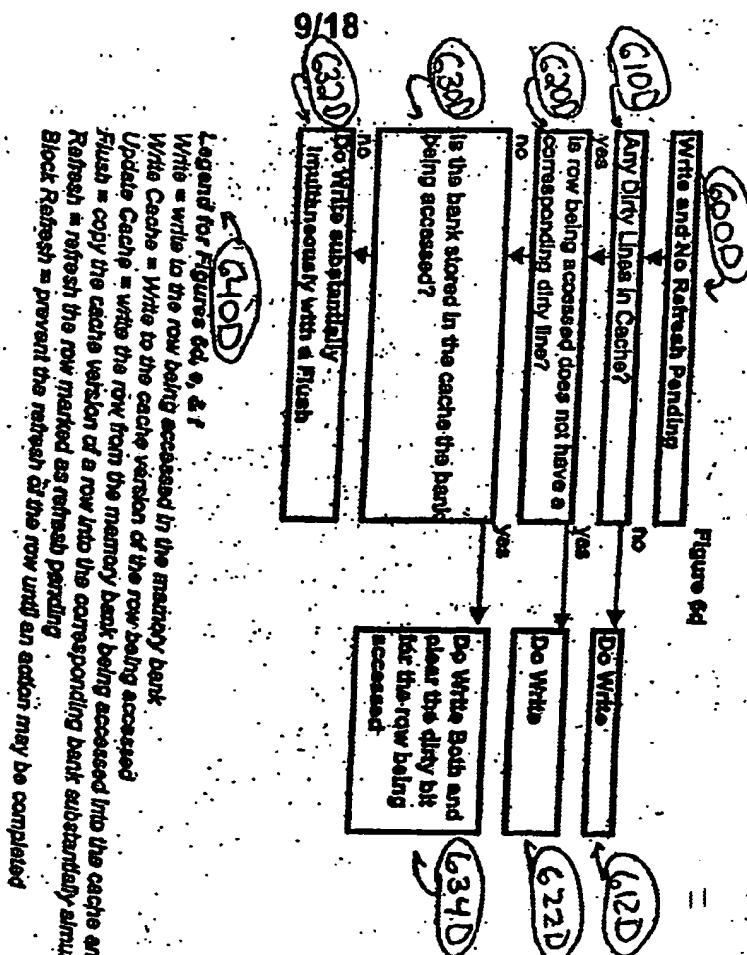


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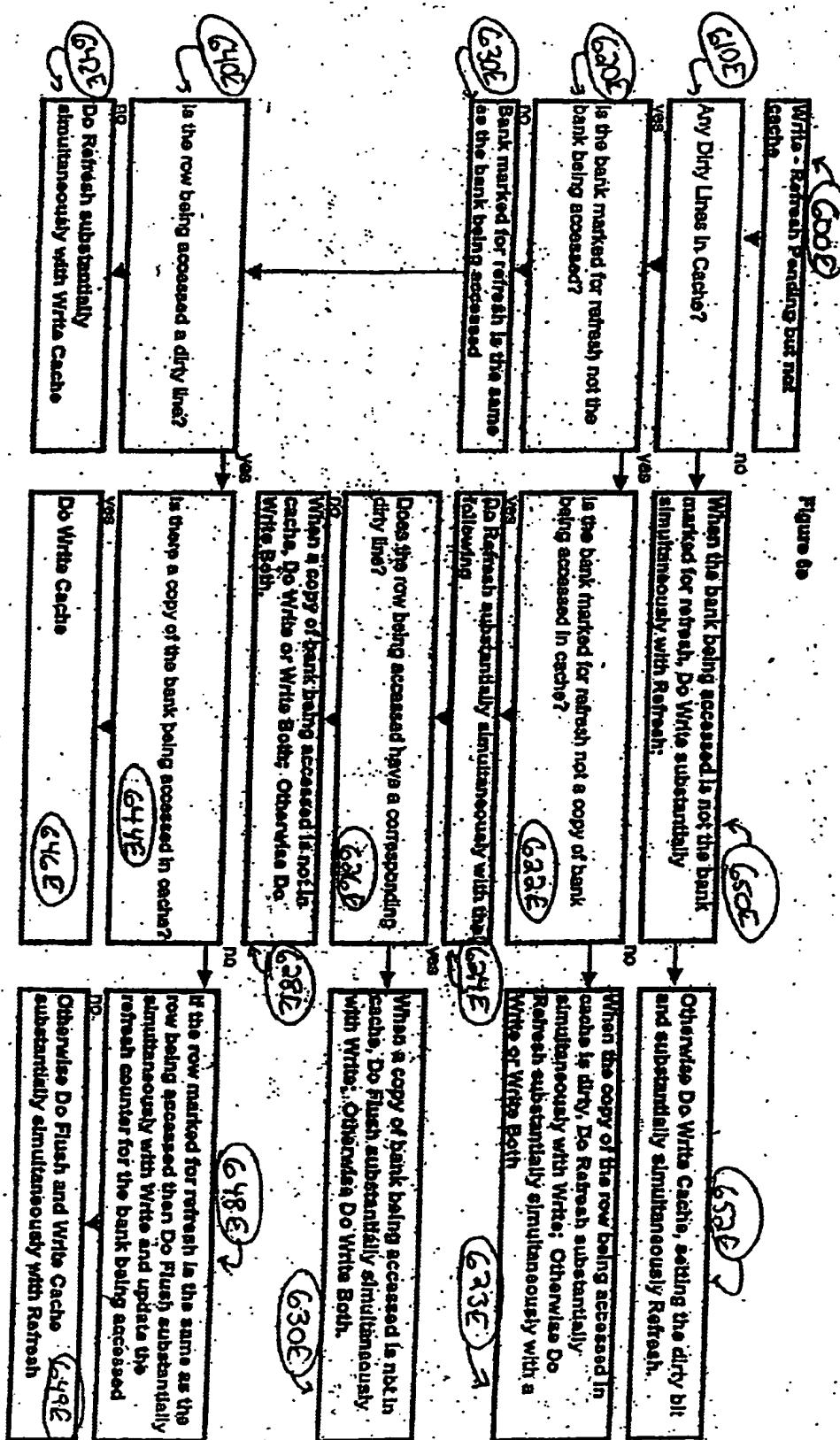


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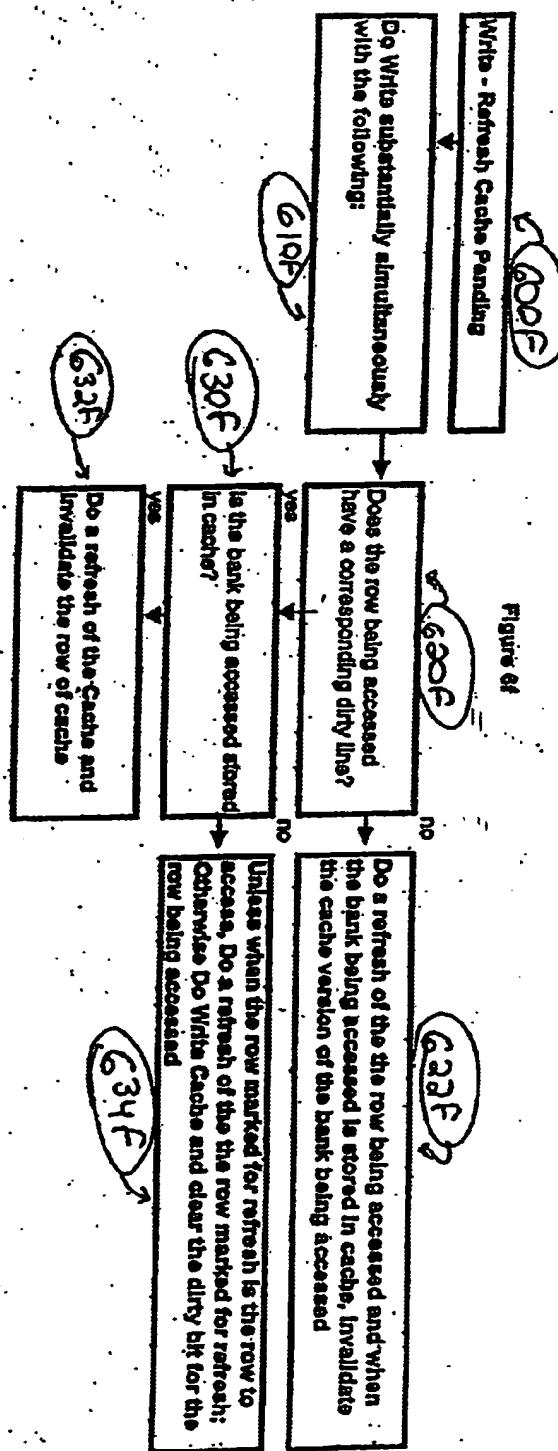
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Figure 7A

Inputs

Refresh Counter: rb, π /* refresh bank, refresh row */
 Current Access Address: wb, wr /* access (write) bank and row */
 Number of rows in a bank: row

Buffers

Valid[row]
 Dirty[row]
 Cache[row]
 Cachetag[row]

/* valid bits for each of the rows in the cache bank */
 /* dirty bits for cache lines */
 /* cache bank */
 /* Tag for cache lines */

Functions

Refresh()
 Flush()
 ReadUpdateCO()
 Read()
 Write()
 ReadCache()
 WriteCache()
 WriteBoth()

{mem[b, r] = mem[b, rr];}
 {mem[cachetag[wr], wr] = cache[wr];} /* SS cache[wr] = mem[wr, wr]; */
 {data_out = mem[wb, wr];}
 {data_out = mem[wb, wr];}
 {mem[wb, wr] = data_in;}
 {data_out = cache[wr];} /* SS cache[wr] = cache[wr]; */
 {cache[wr] = data_in;} /* SS cache[wr] = wb */
 {Write() /* SS WriteCache() */ dirty[wr] = 1;}
 /* write to both the cache and memory */

(SS - means operations are done in parallel)

pseudo program description

/* Initialize all cachetags to be NULL */
 Cachetag[] = NULL;
 /* READ */

/*----- No refresh pending -----*/
 if (no refresh pending) {
 if (no dirty line) {ReadUpdateCO();}
 else /* there is a dirty line */ {
 if (!dirty[wr]) {ReadUpdateCO();}
 else if (wb == cachetag[wr]) {ReadCache() /* SS Flush() */ dirty[wr] = 0;}}

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Figure 7B

```

/* ----- Refresh pending -----*/
else {
  If(rb != cache) {
    If(no dirty line) {
      if(rb == wb) { Read0 $$ Refresh0; }
      else /* rb == wb */
        if(wb == tag[w]) {
          ( ReadCache0 $$ Refresh0; )
        }
    }
    else /* there is a dirty line */
      if(rb == wb) {
        Refresh0 $$ Read0;
        if(tag[w] != wb) {
          if(dirty[w]) { Flush0 $$ Read0; }
          else ReadUpdateCO;
        }
        else {
          if(dirty[w]) { ReadCache0 $$ Flush0; }
          else Read0;
        }
      }
    /* end if rb == wb */
  }
  else /* refresh bank is the same as the accessed bank */
  if(wr == rr) {
    if(tag[w] != wb) {
      if(dirty[w]) { Flush0 $$ Read0
                     $$ UpdateRefreshCounter0; }
      else { ReadUpdateCO $$ Update Refresh Counter0; }
    }
    else {
      if(dirty[w]) { ReadCache0 $$ Flush0
                     $$ UpdateRefreshCounter0; }
      else { ReadUpdateCO $$ Update Refresh Counter0; }
    }
  }
  else {
    if(tag[w] == wb) { Refresh0 $$ ReadCache0;
                       /* dirty status for the line unchanged */
    }
    else {
      BlockRefresh;
      if(dirty[w]) { Flush0 $$ Read0; }
      else ReadUpdateCO;
    }
  }
}

```

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Figure 7C

```
else /* the cache bank is being refreshed */ {
    if (dirty[wr]) {
        if ((tag[wr] == wb) {
            BlockRefresh:
            ReadCache0 $$ Flush0;
        }
        else {
            BlockRefresh;
            Read0 $$ Flush0;
        }
    }
    else {
        Refresh0
        Read0
    }
} /* end refresh pending */
```

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Figure 7D

```
/* *** WRITE ***/  
  
/* ----- No pending refresh ----- */  
if (no refresh pending) {  
    /* there is no dirty line */  
    if (no dirty line) {Write0; }  
    else {  
        /* there is a dirty line */  
        if (!dirty[wr]) { Write0; }  
        else {  
            if (Cachetag[wr] == wb) { WriteBoth0 $$ dirty[wr] = 0; }  
            else {Write0 $$ Flush0; }  
        } /* end dirty line */  
    }  
}
```

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Figure 7E

```
/* ----- Pending refresh -----, */  
else {  
    if(rb != cache) {  
        if(no dirty line) {  
            if(wb == rb) { Write0 $$ Refresh0 )  
            else { WriteCache0 $$ dirty[wr] = 1 $$ Refresh0 ;}  
        }  
        else {  
            /* there is a dirty line */  
            if(rb != wb) { /* refresh bank is different from the access bank */  
                if(rb != cachetag[wr]) {  
                    Refresh0 $$  
                    If(dirty[wr]) {  
                        If(cachetag[wr] != wb) {Flush0 $$ Write0;)  
                    }  
                    else {  
                        If(cachetag[wr] == wb) { Write0; /* or writeboth0 */  
                    Else { Writeboth0;)  
                }  
                else {  
                    if(dirty[wr]) { Refresh0 $$ Write0; /* cache line remains dirty */  
                    else { Refresh0 $$ Write0; /* Or writeboth0 */  
                }  
            }  
            else { /* refresh bank is the same as the access bank */  
                If(dirty[wr]) {  
                    If(cachetag[wr] == wb) { Writecache0;)  
                else {  
                    if(wr == n) { /* lucky day */  
                        Flush0 $$ write0 $$ Updaterefreshcounter;  
                    }  
                    else {  
                        Flush0 and write to cache with new data ;  
                    }  
                }  
            }  
        }  
    }  
}/* the line is not dirty */  
/* create another dirty line */  
Refresh $$  
WriteCache0;  
}
```

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```
else /* cache bank is being refreshed */
Write0 $$

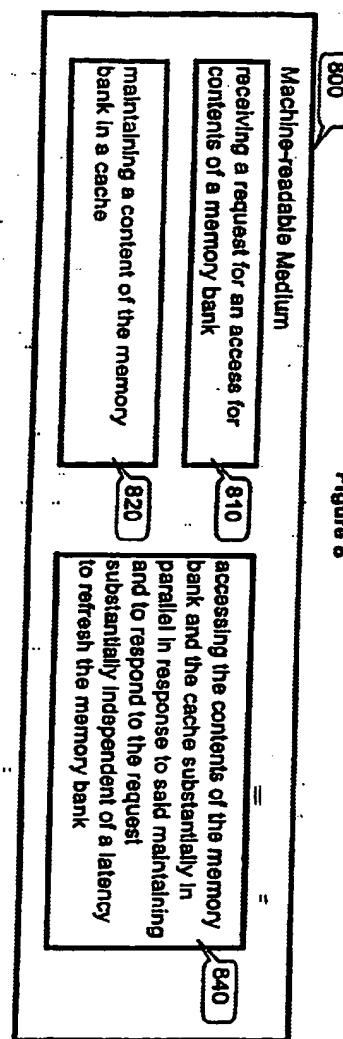
if (dirty[wr]) {
    if (cachetag[wr] == wb) {
        Refresh0 $$

        Cachetag[wr] = NULL;
    }
    else {
        Refresh0;
        /* unless wr = rr then we writeback and clear dirty bit */
    }
}
else /* not dirty */
Refresh0;
if (cachetag[wr] == wb) { Cachetag[wr] = NULL;}
```

Figure 7F

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